



SPAWAR
Systems Center
San Diego

TECHNICAL DOCUMENT 3097
January 2000

Tetra-Methyl Ammonium Hydroxide (TMAH) Preferential Etching for Infrared Pixel Arrays

P. Sullivan
B. W. Offord
M. E. Aklufi

Approved for public release;
distribution is unlimited.

SSC San Diego

20000403 010

TECHNICAL DOCUMENT 3097
January 2000

Tetra-Methyl Ammonium Hydroxide (TMAH) Preferential Etching for Infrared Pixel Arrays

P. Sullivan
B. W. Offord
M. E. Aklufi

Approved for public release;
distribution is unlimited.



SSC San Diego
San Diego, CA 92152-5001

SSC SAN DIEGO
San Diego, California 92152-5001

E. L. Valdes, CAPT, USN
Commanding Officer

R. C. Kolb
Executive Director

ADMINISTRATIVE INFORMATION

The work described in this document was performed for David Taylor Research Center (Code 0116) by the Integrated Circuit Research and Fabrication Branch (D876), SSC San Diego.

Released by
E. P. Kelley, Acting Head
Integrated Circuit Research
Branch

Under authority of
E. A. Engh, Head
Information Assurance
& Engineering Division

CONTENTS

| | |
|---|------------|
| INTRODUCTION | 1 |
| PREFERENTIAL ETCHING AS A METHOD FOR THERMAL ISOLATION | 2 |
| DOPED TMAH IN WATER AS THE ANISOTROPIC ETCHANT | 2 |
| TMAH ETCH EXPERIMENTS, RESULTS, AND OBSERVATIONS..... | 3 |
| EXPERIMENT 1 | 3 |
| Test Sample Preparation | 3 |
| First Etchant Solution | 3 |
| EXPERIMENT 2 | 4 |
| EXPERIMENT 3 | 6 |
| New Test Sample Preparation..... | 6 |
| EXPERIMENT 4 | 7 |
| EXPERIMENT 5 | 9 |
| EXPERIMENT 6..... | 11 |
| REFERENCES..... | 13 |
| APPENDIX A: TMAH ETCHING PROCEDURE AND APARATUS..... | A-1 |

Figures

| | |
|--|----|
| 1. Design layout of thermally isolated resistor and SEM of structure after silicon etch. SEM sample has been cleaved, showing isolation under suspended structure | 1 |
| 2a. 2044a cross section (Experiment 1) | 4 |
| 2b. 2044a ledge close-up (Experiment 1) | 4 |
| 3a. 2044A2 SEM X section (Experiment 2) | 5 |
| 3b. Optical photograph of (111) etch surface taken at 40x (Experiment 2) | 5 |
| 4. 10-minute etch (Experiment 2)..... | 5 |
| 5a. Cross section of Al pad (Experiment 2) | 6 |
| 5b. Tilt view of Al pad (Experiment 2) | 6 |
| 6a. 2214-2 cross section (Experiment 3) | 7 |
| 6b. 2214-2 etch pit (Experiment 3)..... | 7 |
| 7a. 2214-3 (100) etch depth cross section (Experiment 4) | 8 |
| 7b. 2214-3 cross section (Experiment 4) | 8 |
| 8a. 2214-2 backside (Experiment 3) | 9 |
| 8b. 2214-3 backside (Experiment 4) | 9 |
| 9a. 2214-4 (100) etch depth cross section (Experiment 5) | 10 |
| 9b. 2044-4 cross section (Experiment 5) | 10 |
| 10a. 2214-4 SEM backside (Experiment 5) | 11 |
| 10b. 2214-4 optical photograph of etch pit (Experiment 5) | 11 |
| 11a. 2214-4 cross section (Experiment 6) | 12 |
| 11b. 2214-4 etch pit (Experiment 6)..... | 12 |
| 12a. 2044-4 optical 100x photograph of etch pit (Experiment 6) | 12 |
| 12b. 2214-4 SEM backside (Experiment 6) | 12 |

INTRODUCTION

Polysilicon resistors fabricated on silicon substrates and encapsulated in silicon dioxide can be used as infrared (IR) emitters (Parameswaran et al., 1999). Current is passed through these polysilicon emitters and resistor heating generates thermal energy. This thermal energy can be expressed as the square of the current times the resistance of the emitter: $E_t = I^2 R$. This thermal energy is dissipated by two means: (1) infrared radiated energy, and (2) thermal energy conducted away by the substrate or the bulk of the material. For this device to act as an infrared emitter, the radiated energy term must be optimized. This means that the conducted energy term must be minimized. To minimize the conducted energy term, it is desirable to reduce or eliminate the silicon under the polysilicon resistor used as an IR emitter.

An IR scene simulator employs a silicon-based micromachined Complementary Metal Oxide Semiconductor (CMOS) electronic-driven array of these miniature IR heater elements. The concept of the programmable IR pixel array is based upon the suspension of micro-heaters over a micro-machined cavity in the silicon substrate. Each heater is surrounded by pixel-specific electronics that allow rapid loading and data retention. The array is surrounded by data input and pixel address control electronics. The micromachined cavity is constructed by using a silicon etchant that undercuts a desired pattern while leaving it connected to create a suspended structure. The pattern is created by patterning and plasma etching silicon dioxide, thereby exposing the substrate silicon of the CMOS chip. The exposed silicon is then exposed to a silicon anisotropic etchant. Figure 1 shows the design layout and the scanning electron micrograph (SEM) of such a structure.

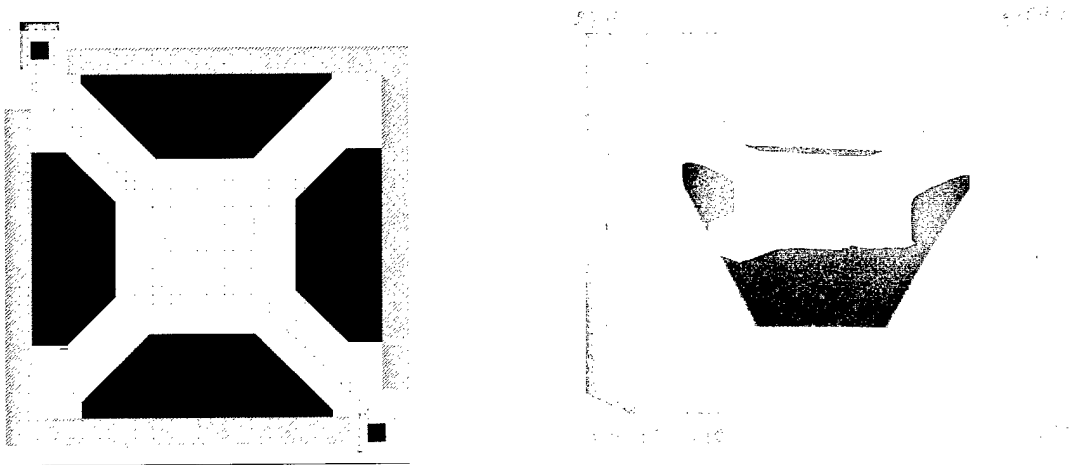


Figure 1. Design layout of thermally isolated resistor and SEM of structure after silicon etch. SEM sample has been cleaved, showing isolation under suspended structure.

PREFERENTIAL ETCHING AS A METHOD FOR THERMAL ISOLATION

To create IR scene generators with sufficient resolution, many of these heaters must be produced in an array. For a cost-effective approach, these arrays must be small and mass-produceable. A CMOS/microelectromechanical systems (MEMS) approach to creating these scene generators was chosen as cost effective. The CMOS electronics are produced at a commercial or otherwise standard foundry, and the resultant wafers are put through the post-processing etch step to create monolithic thermal pixel arrays (TPAs). A post-processing etch must completely isolate the heaters and not affect the CMOS electronics in any way. An isotropic etch of silicon would create too much of an undercut of the CMOS pixel control electronic, so a crystallographic etch is required. The silicon etchant used was a tetra-methyl ammonium hydroxide (TMAH) solution. Potassium hydroxide (KOH) and ethylene diamine pyrocatechol (EDP) can also be used as crystallographic etches of silicon; however both are hazardous, and KOH attacks metal, which would remove metal from bonding pads on the CMOS chip. TMAH was chosen for the following reasons: (1) it is commonly used to etch silicon wafers, (2) it is not as hazardous as the other etchants, being just concentrated photoresist developer used in our laboratory for semiconductor processing, (3) literature suggests that a solution could be made with TMAH that did not attack metal, and (4) it is readily available. Appendix A lists the proper procedure and chemical solution for this etch.

DOPED TMAH IN WATER AS THE ANISOTROPIC ETCHANT

TMAH solutions in water are highly desirable as an anisotropic etch for micromachining silicon wafers that have completed integrated circuit fabrication. Specifically, 5% (by weight) TMAH solutions in water at 80°C exhibit 20:35:1 etch ratios for the (100):(110):(111) crystal planes respectively (Tabata et al., 1992) with the etch rate of the (100) plane at approximately 0.7 to 0.8 $\mu\text{m}/\text{min}$. Additionally, solutions of TMAH in water exhibit high selectivity between silicon passivation layers such as SiO_2 (selectivity between thermal SiO_2 and (100) Si at $(5.3\text{e}3):1$, at 5wt% 80°C) and Si_3N_4 (selectivity between LPCVD Si_3N_4 and (100) Si at $24.4\text{e}3:1$, at 5wt% 80°C) (Schnakenberg, Benecke, and Lange, 1991). Thus, these passivation layers are excellent candidates to use as etch masks. TMAH solutions doped with silicon can reduce or eliminate the etching of exposed aluminum integrated circuit bonding pads during the silicon etch process (Tabata et al., 1992; Schnakenbaerg et al., 1991). TMAH solutions doped with silicon also increase the selectivity between silicon and passivation layers such as SiO_2 by a factor of 4 to 7, and Si_3N_4 by a factor of 2 without reducing the etch rate of Si (Schnakenberg et al., 1991).

One of the problems that has been observed with etching silicon with doped and undoped TMAH and water solutions is that of crystal hillock formation on the (100) plane during the etch process (Tabata et al., 1992; Schnakenberg et al., 1991). This crystal hillock formation reduces the etch rate of the (100) crystal plane, and occurs for solution concentrations below 20 to 22 wt%. Orange-peel-like surfaces are observed for concentrations above 20 to 22 wt%, with a corresponding increase in the (100) etch rate (Tabata et al., 1992; Schnakenberg et al., 1991). This crystal hillock formation can be repressed in lower concentration solution (around 5%) by

the addition of strong oxidizers such as ammonium persulfate $[(\text{NH}_4)_2\text{S}_2\text{O}_8]$ or potassium persulfate $(\text{K}_2\text{S}_2\text{O}_8)$ (Klaassen et al., 1996).

TMAH ETCH EXPERIMENTS, RESULTS, AND OBSERVATIONS

The method of doping the TMAH and water solution with silicon used in these experiments follows that of Klaassen et al. (1996) and uses silicic acid (H_2SiO_3) as the silicon doping source and ammonium persulfate $[(\text{NH}_4)_2\text{S}_2\text{O}_8]$ as the strong oxidizer.

The purpose of the following experiments was to repeat and improve upon work performed by Optical E.T.C. Inc. under SPAWAR Systems Center, San Diego, contract number N66001-95-C-0033, and reported under CDRL B004¹. Specifically, this work provided mixing procedures that produced solutions that had to be discarded regularly. This occurred because sometimes the additives did not dissolve, thus producing cloudy solutions. In other words, cloudy and clear solutions were produced irregularly using the same mixing procedure.

EXPERIMENT 1

Test Sample Preparation

Six-inch silicon wafers were thermally oxidized ($\approx 7650\text{\AA}$). This oxide was patterned by photolithographic techniques followed by a buffered hydrofluoric acid oxide etch and photoresist strip. These samples were sawed into $\frac{1}{4}$ wafers. These $\frac{1}{4}$ wafers were dipped in pad etch for 20 sec and then rinsed in de-ionized (DI) water immediately before TMAH etching to remove native oxide that could inhibit silicon etching.

First Etchant Solution

Formula: assumption: 25% TMAH in H_2O by volume = 25% TMAH by weight

A 400-ml 25% TMAH solution was combined with 63 g of silicic acid. Magnetic stirring was applied for a half-hour. This solution turned to a gel and the magnetic stirrer stopped sometime during this half-hour. An additional 150-ml 25% TMAH was added to this and the gel dissolved. Then, 1600 ml of DI water was added. Some gel reformed at the bottom of the beaker. This solution was heated to 80°C while stirring magnetically at 60 rpm. The temperature of the solution was controlled by using a Resistance Temperature Detector (RTD) in the solution and a Proportional Integral Differential (PID)-controlled hot plate. The solution took approximately 1 hour to heat. Then, 10 grams of ammonium persulfate was added directly to hot solution. The ammonium persulfate clumped up at this time. Approximately 45 minutes later, the sample as prepared above was added to the solution. The solution still had clumps (smaller) of ammonium persulfate as described above at this time. This sample was etched for 2 hours and 5 minutes. When the sample was removed from the etchant, no clumps of ammonium persulfate were observed. Figures 2a and 2b show the result of etching this sample.

¹ Optical E.T.C. 1998. "Real-Time Infrared Test Set." Contract Number N66001-95-C0033, CDRL B004.

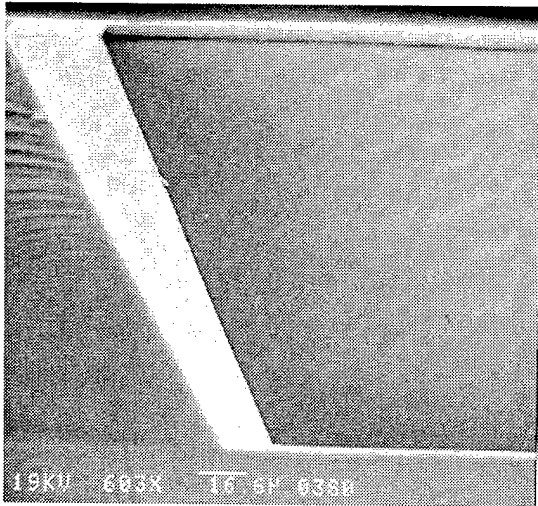


Figure 2a. 2044a cross section (Experiment 1).

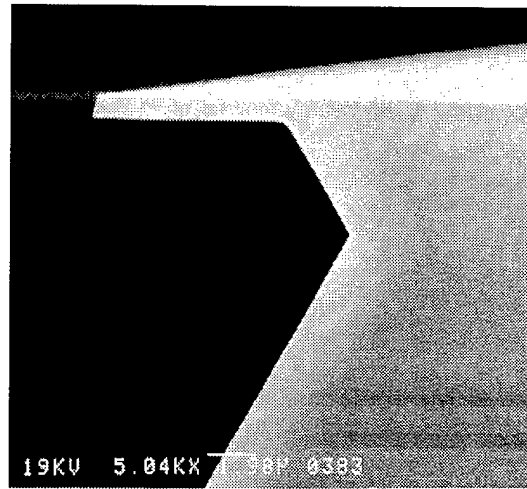


Figure 2b. 2044a ledge close-up (Experiment 1).

Wafer 2044A shows an etch depth (100) of 122.01 μm for a 125-minute etch time. This computes to an etch rate of 0.98 $\mu\text{m}/\text{minute}$ for the (100) silicon plane. This is considerably faster than that reported in the literature for a 5% solution. No crystalline hillocks were observed in this sample. A close-up of the oxide ledge (figure 2b) shows an undercut of the oxide exposing two (111) facets of the silicon. If the distance between the edge of the oxide ledge and the extrapolated line between the lower facet and the oxide silicon interface is measured, the etch rate of the (111) plane can be measured.

$$(111) \text{ material etched} = (6.8 \text{ cm} * 1.98 \mu\text{m}/\text{cm})\sin(54^\circ) = 10.9 \mu\text{m}$$

$$(111) \text{ etch rate} = (10.9 \mu\text{m})/125 \text{ minutes} = 0.0872 \mu\text{m}/\text{min}$$

$$\text{etch ratio} = (100)/(111) = 11.24:1$$

EXPERIMENT 2

Experiment 2 had two objectives: (1) mix a 5% solution of TMAH in H_2O , add 16 g/l silicic acid to a 5% solution and measure etch rate of exposed aluminum, and (2) add 7 grams of ammonium persulfate to this solution without the clumping observed in experiment 1 to prevent crystal hillock formation during etch.

Adding 340 ml of 25% TMAH in H_2O (total) to 1.2 L H_2O yielded a 5.6% solution.

Combining 300 ml of 25% TMAH solution with 67 grams of silicic acid (36% silicon by weight = 24 grams of silicon) turned the solution to a gel. Then 1200 ml of DI water was added. Some gel remained at the bottom of the beaker. This solution was swirled in the beaker to assist in dissolving the gel. It was placed on a hot plate and a magnetic stirrer was applied at 100 rpm and the solution was heated to 80°C while constantly stirring. The temperature of the solution was controlled by using a RTD in the solution and a PID-controlled hot plate. The solution took approximately 1 hour to heat. The solution was clear after reaching a temperature of 80°C. When 7 grams of ammonium persulfate was dissolved in 40 ml of 25% TMAH, and added directly to hot solution, no clumping of the ammonium persulfate was observed. Approximately 30 minutes later, the sample as prepared and described in Experiment 1 above was added to the solution. In addition, die IRTA1 was dipped in

pad etch for 20 sec, rinsed, and added to the solution as described above at the same time. These samples were etched for 55 minutes and then rinsed in DI water for 5 minutes. Figure 3a and 3b show the result of etching this sample. Immediately after removing first ¼ wafer and sample IRTA1 from the etching solution, another wafer was prepared as described above and etched for 10 minutes. Figure 4 shows the result of etching this sample.

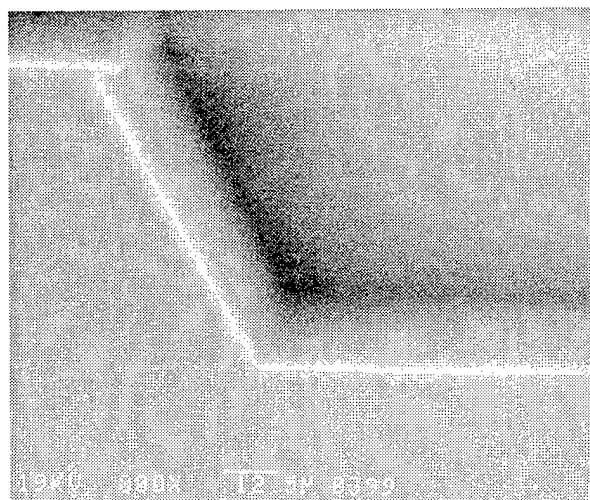


Figure 3a. 2044A2 SEM X section (Experiment 2).

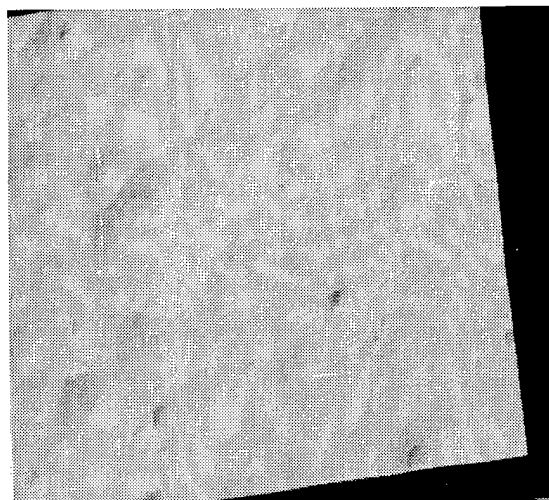


Figure 3b. Optical photograph of (111) etch surface taken at 40x (Experiment 2).

Figure 3a (Wafer 2044A2) shows a (100) etch depth of 57.5 μm for a 55-minute etch. This computes to an etch rate of 1.05 $\mu\text{m}/\text{minute}$ for the (100) silicon plane. No crystalline hillocks were observed in this sample, as figure 3b shows. Figure 3b shows the typical orange-peel-like surface representative of etching with no crystal hillock formation on the (111) etch surface.

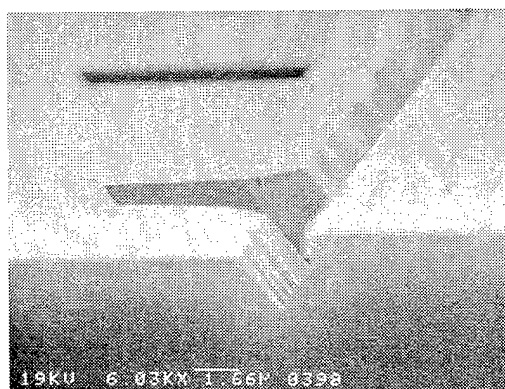


Figure 4. 10-minute etch (Experiment 2).

As figure 4 shows, the results of the 10-minute etch indicates irregular etching. This sample exhibits trenching next to the oxide step, and pitting in the field of exposed silicon. It is assumed that this is caused by a small amount of native oxide over the exposed silicon, causing an activation time

for etching the exposed silicon that is greater than 10 minutes. In addition, it can be postulated from the observed trenching next to the oxide step that this step increases wetting of the silicon in the adjacent area because of the hydrophilic nature of the silicon dioxide and the increased surface area in this region. Therefore, it can be assumed that the addition of a surfactant may decrease the activation time and make the etch more uniform.

Figures 5a and 5b show the a cross section through an aluminum (Al) pad of the sample RTIR1 that was etched at the same time as the $\frac{1}{4}$ wafer in figures 3a and 3b. This demonstrates that little to no aluminum was etched during this procedure.

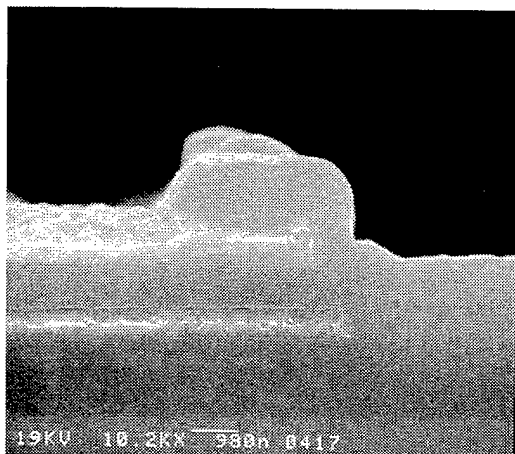


Figure 5a. Cross section of Al pad (Experiment 2).

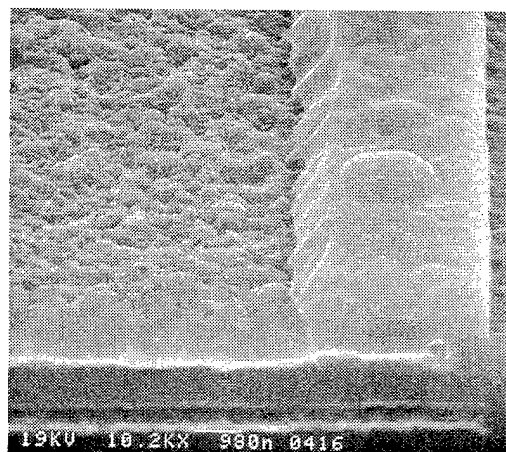


Figure 5b. Tilt view of Al pad (Experiment 2).

EXPERIMENT 3

New Test Sample Preparation

Six-inch silicon wafers (Lot 2214) had 3.0- μm PECVD oxide deposited on bulk test wafers (3.2 to 3.5 μm measured). This oxide was patterned by photolithographic techniques followed by a buffered oxide etch and photoresist strip. One of these wafers was sawed into quarters. A $\frac{1}{4}$ wafer was dipped in pad etch for 20 sec and then rinsed in DI water immediately before TMAH etching to remove native oxide that could inhibit the silicon etching.

In addition, a 6-inch silicon wafer containing thermal pixel arrays designed at SPAWAR Systems Center, San Diego (SSC San Diego) and fabricated at Supertex, Inc. was cut into quarters. This wafer had thick-patterned passivation exposing the silicon to be etched. This $\frac{1}{4}$ wafer was dipped in pad etch for 20 sec and then rinsed in DI water immediately before TMAH etching to remove native oxide that could inhibit the silicon etching.

The third experiment had one objective: to repeat previous results from Experiment 2 on a product wafer. An etch of 90 minutes was used to clear both the larger and the smaller pixel arrays contained on the Supertex wafer.

The solution was mixed as explained in the second experiment, and etched for 90 minutes. Figures 6a and 6b show the result of this etch on 2214-2.

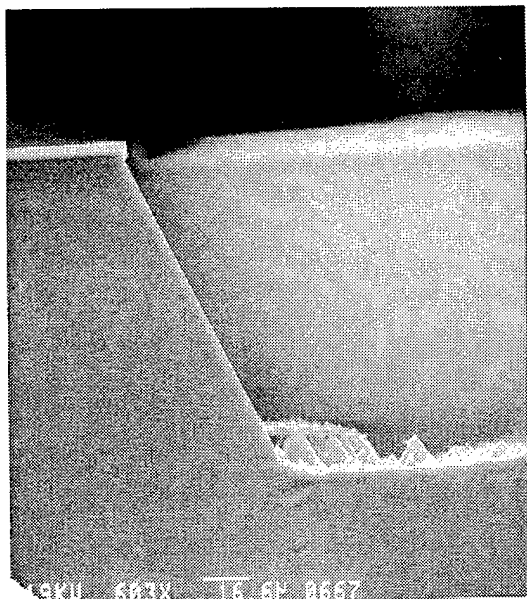


Figure 6a. 2214-2 cross section (Experiment 3).

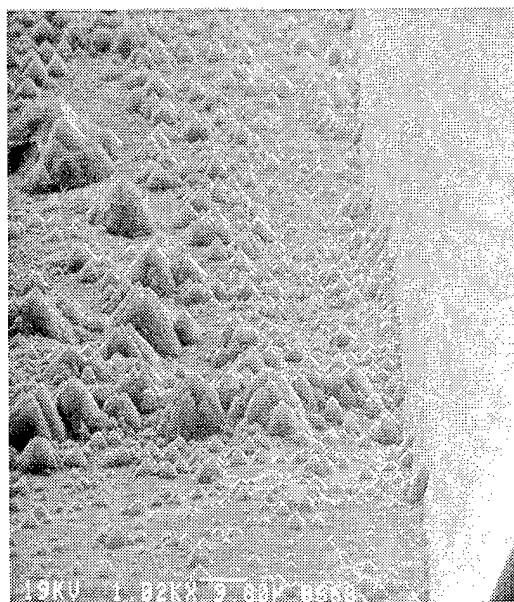


Figure 6b. 2214-2 etch pit (Experiment 3).

Figure 6a (Wafer 2214-2) shows an etch depth of between 68 μm (top of hillocks) to 83 μm (base of hillocks) for the 90-minute etch. This gives an etch rate between 0.76 to 0.92 $\mu\text{m}/\text{min}$. The figure 6b view shows a very rough surface with crystalline hillock formation on the 100 planes. The IR pixels on the Supertex wafer were not all completely isolated, indicating a very nonuniform etch. In addition, the Supertex wafer had particulate contamination all over the wafer. It appeared that oxide from the silicon etch windows broke off and redeposited on the wafer during the etch process. Wafer 2214-2 did not show this contamination.

It was postulated that the amount of ammonium persulfate that was added was on the edge of a process window. It was decided the 3 grams of additional ammonium persulfate would be added on the next run to investigate this possibility.

EXPERIMENT 4

This experiment had one objective: to determine if additional ammonium persulfate in solution would prevent crystal hillock formation during the 90-minute etch process.

A $\frac{1}{4}$ wafer from Lot 2214 and a $\frac{1}{4}$ wafer from the Supertex product lot were used for this investigation. Both wafers were etched for 20 seconds in pad etch, and rinsed in DI water for 2 minutes immediately before immersion in the TMAH solution.

The solution was mixed as explained in the second experiment, with the exception that 10 grams (instead of 7 grams) of ammonium persulfate was dissolved in 40 ml of 25% TMAH and added to the hot TMAH-silicic acid solution. The wafers were etched for 98 minutes, after which they were rinsed in DI water for 15 minutes. Figures 7a and 7b show the result of this etch on Wafer 2214-3.

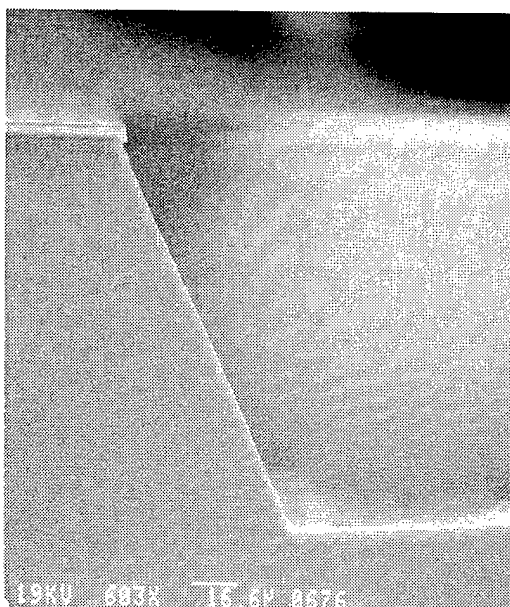


Figure 7a. 2214-3 (100) etch depth cross section (Experiment 4).

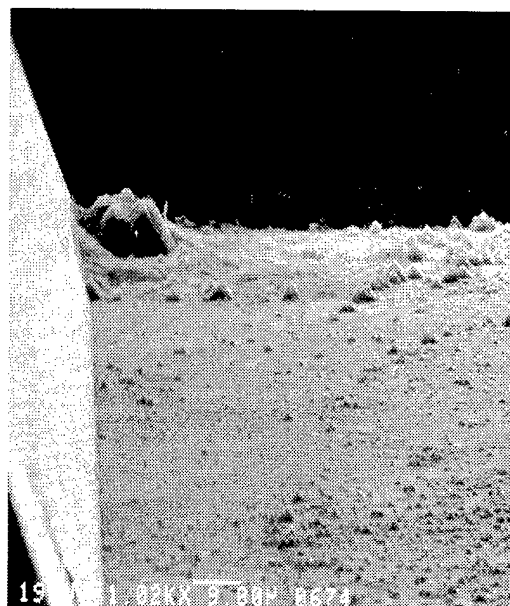


Figure 7b. 2214-3 cross section (Experiment 4).

It was observed that the crystalline hillock formation occurred on both Wafer 2214-3 (as figures 7a and 7b show) and the Supertex wafer; however, the infrared pixels on the Supertex wafer were completely isolated. In addition, the crystalline hillock formation was not as severe as that observed in Experiment 3. Figure 7a (Wafer 2214-3) shows a (100) etch depth of 90 to 98 μm , giving an overall etch rate of 0.92 to 1.00 $\mu\text{m}/\text{min}$ for Experiment 4.

Because of the continued observation of crystal hillocks, an investigation into the difference between the wafers used in Experiments 3 and 4 (lot 2214 and Supertex wafers) and those used in Experiments 1 and 2 (lot 2044) was conducted. The difference was that lot 2044 had a thermal oxide and, thus, had oxide on the backside of the wafer during the TMAH etch. Lot 2214 had a deposited PECVD oxide, which provides little or no backside silicon protection. The Supertex wafers had all gone through back grinding before receipt, providing no backside wafer protection. The backsides of lot 2044, 2214, and the Supertex wafers were inspected from Experiments 1, 2, 3, and 4. No backside etching was observed on the lot 2044 wafer from Experiments 1 or 2.

Backside etching was observed on Wafer 2214-2 and the Supertex wafer from Experiment 3. Wafers from Experiment 3 had severe crystalline hillock formation, and the backside of these wafers appeared to have a "flat" finish. Figure 8a shows the backside of Wafer 2214-2. Wafers from Experiment 4 (Wafer 2214-3) appeared to have less backside etching, with some spots showing a mirrored orange-peel surface with limited hillock formation. Figure 8b shows the backside of Wafer 2214-3. The relative magnifications of figures 8a and 8b are different. The marker in figure 8a shows 2.46 μm while that in figure G2 shows 1.66 μm . Therefore, the crystalline hillock formation in Experiment 4 is much less severe than that observed in Experiment 3.

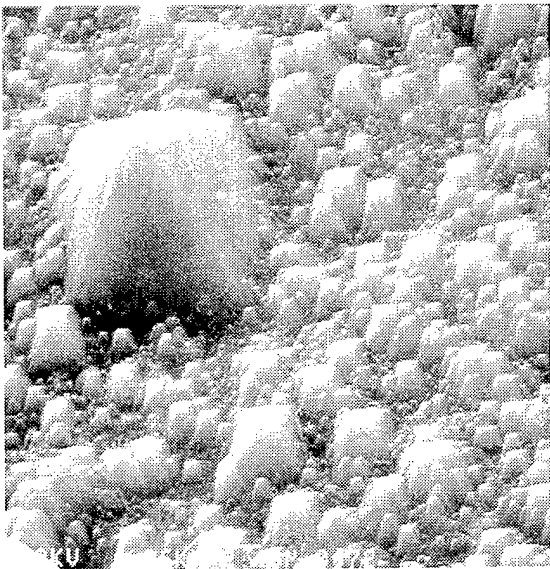


Figure 8a. 2214-2 backside
(Experiment 3).

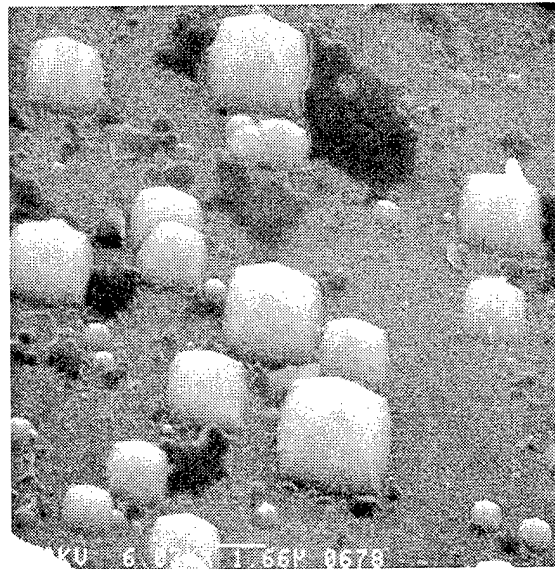


Figure 8b. 2214-3 backside
(Experiment 4).

It was postulated that the effectiveness of the ammonium persulfate against the crystalline hillock formation was related to the amount of silicon etched during this process. The formation of crystalline hillocks has the effect of significantly reducing the etch rate. Therefore, this theory would imply that sometime during the etch, the ammonium persulfate would become extinguished, crystalline hillocks would form, and the etch rate would slow down. Therefore, one of three things need to be done to have a successful etch on these samples: (1) the backside of these wafers would need to be protected, (2) more ammonium persulfate would need to be added to the solution, or (3) these samples would need to be etched for less time.

Given the greatest etch depths measured from the front side etch pits in Experiments 3 and 4, the approximate volume of silicon etched from the backsides of these wafers can be determined as follows:

$$\text{Experiment 3: } 2^{*}(\frac{1}{4}) \pi (3\text{in} * 2.54\text{cm/in})^2 (83 \mu\text{m} * 1\text{e-}4 \text{ cm}/\mu\text{m}) = 0.252 \text{ cm}^3$$

$$\text{Experiment 4: } 2^{*}(\frac{1}{4}) \pi (3\text{in} * 2.54\text{cm/in})^2 (98 \mu\text{m} * 1\text{e-}4 \text{ cm}/\mu\text{m}) = 0.298 \text{ cm}^3$$

EXPERIMENT 5

The objective of this experiment was to determine if a correct amount of ammonium persulfate could be found that would compensate for backside etching of lot 2214 and the Supertex samples.

To assist in this investigation, the maximum amount of ammonium persulfate that could be dissolved in 40 ml of 25% TMAH needed to be found. It was determined that at least 14 grams of ammonium persulfate could be dissolved in 40 ml of 25% TMAH.

A $\frac{1}{4}$ wafer from lot 2044 (backside protected) and a $\frac{1}{4}$ wafer from lot 2214 (backside unprotected) were used for this experiment. Both wafers were etched for 20 seconds in pad etch, and rinsed in DI water for 2 minutes immediately before immersion in the TMAH solution.

The solution was mixed as explained in the second experiment, with the exception that 14 grams (instead of 7 grams) of ammonium persulfate was dissolved in 40ml of 25% TMAH and added to the hot TMAH silicic acid solution. The wafers were etched for 90 minutes, after which they were rinsed in DI water for 15 minutes. Figures 9a and 9b show the results from this etch on lot 2214-4.

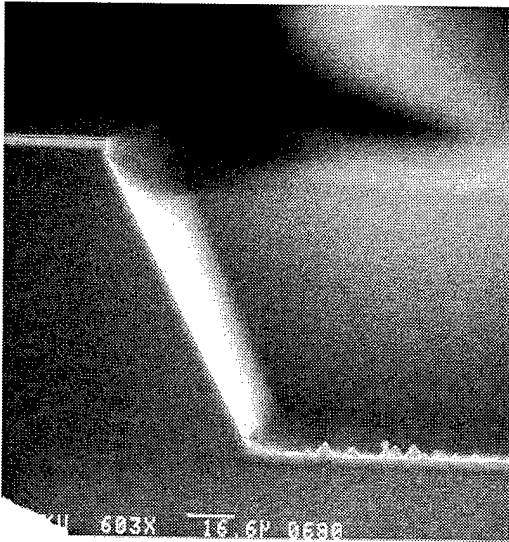


Figure 9a. 2214-4 (100) etch depth cross section (Experiment 5).

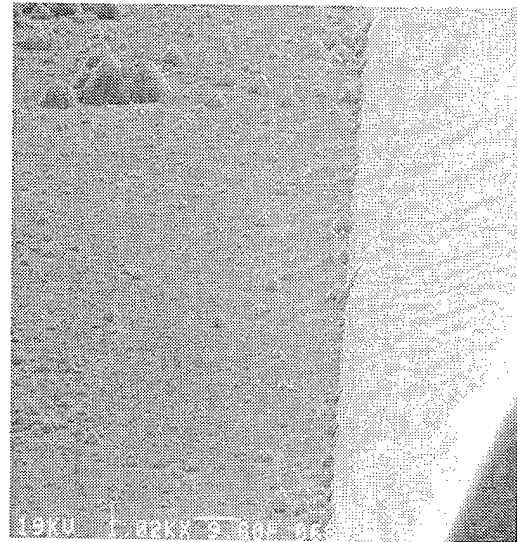


Figure 9b. 2214-4 cross section (Experiment 5).

Slight crystalline hillock formation occurred on both 2044 and 2214-4 wafers. Wafer 2214-4 (figure 9a) shows a (100) etch depth of 78 to 83 μm , giving an overall etch rate of 0.87 to 0.92 $\mu\text{m}/\text{min}$. Backside silicon was etched only from Wafer 2214, giving a volume of etched silicon from the backside at 0.126 cm^3 . This experiment shows that 14 grams is close to compensating for dissolved silicon from a single $\frac{1}{4}$ wafer that experiences backside silicon etching for 90 minutes.

Figure 10a shows an SEM of the backside of wafer 2214-4. The scale marker indicates 980 nm. Figure 10b shows an optical photograph taken at 40x. These figures clearly indicate that additional ammonium persulfate reduces crystal hillock formation caused by large amounts of silicon being dissolved from the backside of the wafer during the etch process.

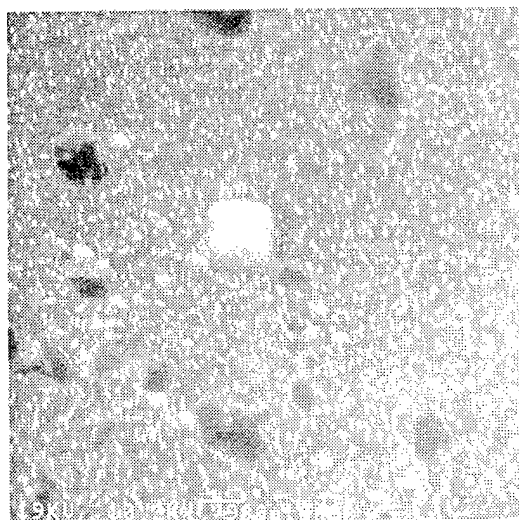


Figure 10a. 2214-4 SEM backside (Experiment 5).

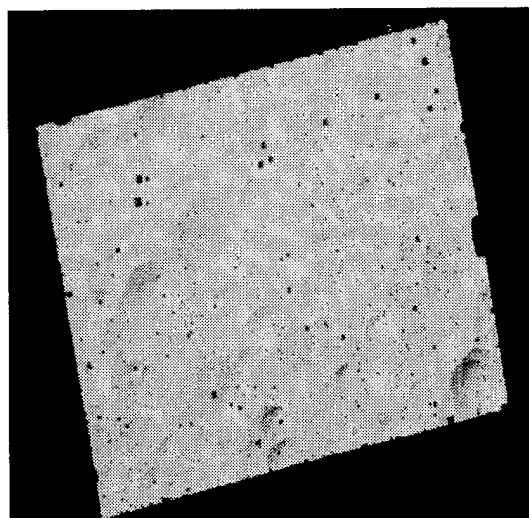


Figure 10b. Optical photograph, etch pit (Experiment 5).

EXPERIMENT 6

The objective of this experiment was to add additional ammonium persulfate to completely compensate for backside etching of Lot 2214 and the Supertex samples. It was determined that at least 21 grams of ammonium persulfate could be dissolved in 40 ml of 25% TMAH.

A $\frac{1}{4}$ wafer from lot 2214 (backside unprotected) was used for this experiment. This wafer was etched for 20 seconds in pad etch, and rinsed in DI water for 2 minutes immediately before immersion in the TMAH solution.

The solution was mixed as explained in the second experiment, with the exception that 21 grams (instead of 7 grams) of ammonium persulfate was dissolved in 40 ml of 25% TMAH and added to the hot TMAH silicic acid solution. The wafers were etched for 90 minutes, after which they were rinsed in DI water for 15 minutes. Figures 11a and 11b show the results from this etch on Wafer 2214-4.

Very slight crystalline hillock formation occurred on the wafer that was etched in this experiment. Figure 11a shows an etch depth of $91\text{ }\mu\text{m}$, giving an overall etch rate of $1.0\text{ }\mu\text{m/min}$. Backside silicon etched from this wafer was 0.137 cm^3 . This experiment shows that compensation of backside silicon etching nearly compensated with 21 grams of ammonium persulfate.

Figure 12a shows an optical photograph of an Experiment 6 etch pit at 100x. This shows an etch surface nearly free from crystal hillock formation. Figure 12b shows an SEM of the backside wafer surface. This SEM shows that all crystal hillocks are less than $1\text{ }\mu\text{m}$ in diameter.

Experiment 6 shows crystal hillocks that are in the nucleation stage. Therefore, this will be set as the minimum ammonium persulfate for a 90-minute etch when a single $\frac{1}{4}$ wafer is etched with exposed silicon on the backside.

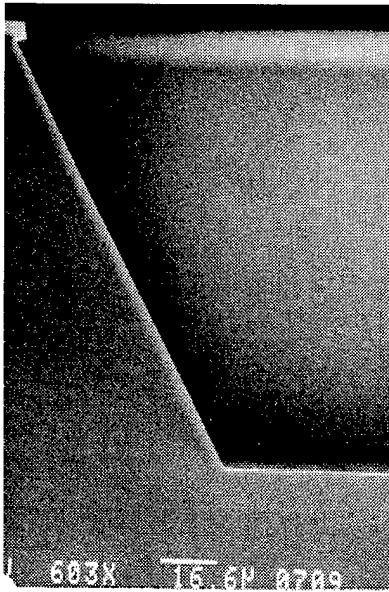


Figure 11a. 2214-4 cross section (Experiment 6).

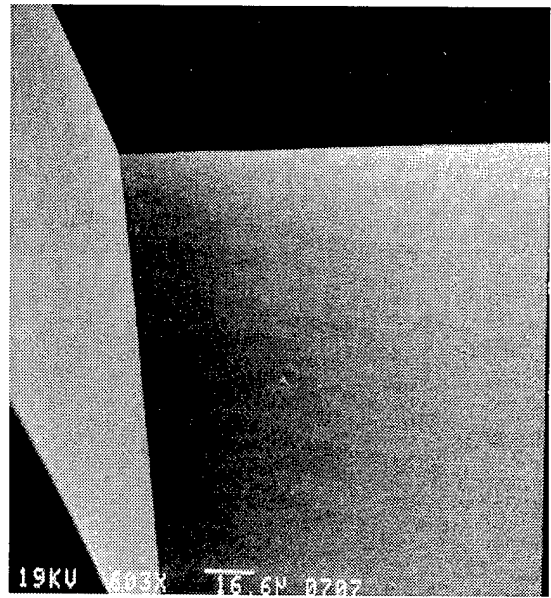


Figure 11b. 2214-4 etch pit (Experiment 6).

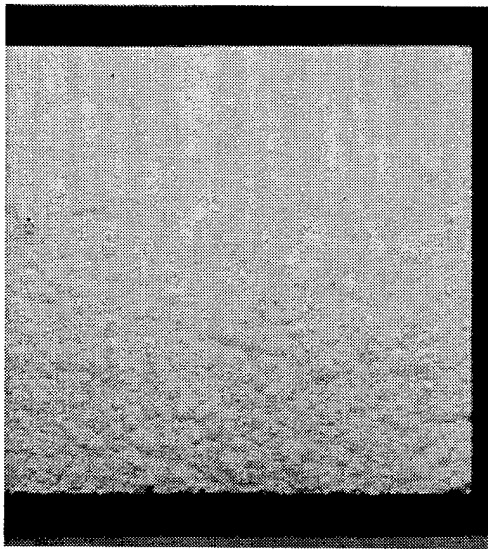


Figure 12a. Optical 100x photograph of etch pit (Experiment 6).

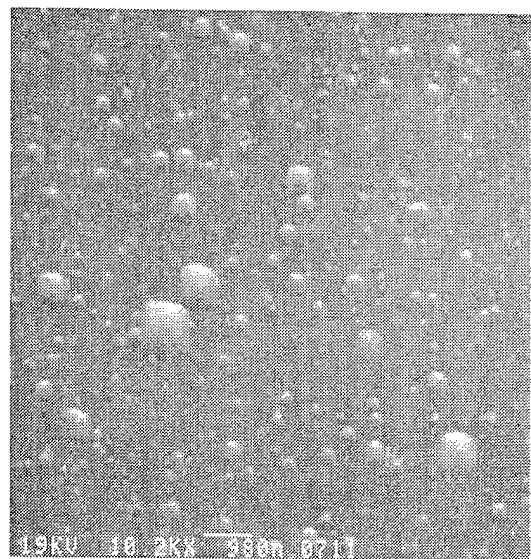


Figure 12b. 2214-4 backside SEM.

REFERENCES

- Klaassen, E., R. J. Reay, C. W. Storment, J. Audy, P. Henry, A. P. Brokaw, and G. T. A. Kovacs. 1996. "Micromachined Thermally Isolated Circuits," *Solid-State Sensor and Actuator Workshop*, Hilton Head, SC, 2-6 June, pp. 127-131.
- Parameswaran, M., A. M. Robinson, D. L. Blackburn, M. Gaitan, and J. Geist. 1991. "MicroMachined Thermal Radiation Emitter from a Commercial CMOS Process," *IEEE Electron Device Letters*, vol. 12, no. 2 (Feb), pp. 57-59.
- Schnakenberg, U., W. Benecke, and P. Lange. 1991. "TMAHW Etchants for Silicon Micromachining." In *Proceedings, Transducers '91, Dig Tech Papers*, San Francisco, CA, pp. 815-818.
- Tabata, O., R. Asahi, H. Funabashi, K. Shimaoka, and S. Sugitama. 1992. "Anisotropic Etching of Silicon in TMAH Solutions," *Sensors and Actuators*, A.34, pp. 51-57.

APPENDIX A

TMAH ETCHING PROCEDURE AND APARATUS

EQUIPMENT

1. Weight Measurement: Scale OHAUS Explorer Electronic Scale
2. Hot Plate/Stirrer: PMC 730 Series Data Plate, Digital Hot Plate/Stirrer
3. Remote Control: PC 740 Controller
4. Etch Container: 2000 ml quartz container with water cooled cover
5. Liquid measuring container: 2000-ml pyrex beaker
6. Solids measuring, tall container: 180-ml aspect ratio pyrex beaker
7. Solids measuring short container: 50 ml pyrex beaker
8. Spoon spatula

CHEMICALS

1. Silicic Acid, $\text{SiO}_2 \cdot 2\text{H}_2\text{O}$ (H_2SiO_3)
2. TMAH, tetra-methyl ammonium hydroxide, $(\text{CH}_4)_4 \text{NOH}$
3. Ammonium persulfate, $(\text{NH}_4)_2 \text{S}_2\text{O}_8$

ETCH SOLUTION PREPARATION

Preparation to be performed in vented hood/sink.

Solution A

- A1. Place teflon-coated magnetic stirrer into a clean dry 2000-ml etch container.
- A2. Place on hot plate stirrer.
- A3. Weigh out approximately 50-gms of silicic acid into 180-ml beaker, note the weight and add to etch container.
- A4. Weigh out additional silicic acid to bring the total silicic acid to 67 gms (approximately 17 grams) and add to etch container.
- A5. Measure out 300 ml of 25% TMAH into 2000-ml pyrex beaker, and add to etch container.
- A6. Measure 1200 ml of DI water into 2000-ml pyrex beaker, and add to etch container.
- A7. Swirl 2000-ml etch container until silicic acid dissolves.
- A8. Place condensor unit and temperature probe in location and start water flow through condensor.
- A9. Set remote stirrer to 200 rpm; set probe temperature to 80°C. Solution will be cloudy.

A10. Solution will clear in approximately 1 hour when it reaches 80°C.

Solution B

- B1. Measure 7 grams of ammonium persulfate into the 50-ml pyrex beaker.
- B2. Measure 40 ml of 25% TMAH and place in another 50-ml pyrex beaker.
- B3. Add the 7 grams of ammonium persulfate to the 50-ml pyrex beaker containing the 40 ml of TMAH and stir to completely dissolve ammonium persulfate.
- B4. Pour TMAH-ammonium persulfate solution into etch container after the TMAH-silicic acid solution reaches 80°C.
- B5. Wait 30 minutes for solution to stabilize before etching material.

The method described above gives an estimated etch rate of 1 $\mu\text{m}/\text{min}$ for small volumes of silicon removed.

REPORT DOCUMENTATION PAGEForm Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

| | | | |
|--|---|---|--|
| 1. AGENCY USE ONLY (Leave blank) | | 2. REPORT DATE January 2000 | 3. REPORT TYPE AND DATES COVERED Final |
| 4. TITLE AND SUBTITLE TETRA-METHYL AMMONIUM HYDROXIDE (TMAH) PREFERENTIAL ETCHING FOR INFRARED PIXEL ARRAYS | | 5. FUNDING NUMBERS PE: 0603712NM AN: DN305061 WU: EE97 | |
| 6. AUTHOR(S) P. Sullivan, B. W. Offord, M. E. Aklufi | | 8. PERFORMING ORGANIZATION REPORT NUMBER TD 3097 | |
| 7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) SSC San Diego San Diego, CA 92152-5001 | | 10. SPONSORING/MONITORING AGENCY REPORT NUMBER | |
| 9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) David Taylor Research Center Code 0116 Bethesda, MD 20084 | | | |
| 11. SUPPLEMENTARY NOTES | | | |
| 12a. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution is unlimited. | | 12b. DISTRIBUTION CODE | |
| 13. ABSTRACT (Maximum 200 words) An infrared scene simulator employs a silicon-based micromachined Complementary Metal Oxide Semiconductor (CMOS) electronic-driven array of miniature infrared heater elements. The IR pixel array is based upon the suspension of micro-heaters over a micromachined cavity in the silicon substrate. A polysilicon resistor is used as the infrared emitter. To create IR scene generators with sufficient resolution, a large number of micro-heaters need to be produced in an array. A CMOS/microelectromechanical systems (MEMS) approach to creating these scene generators was chosen as cost effective. The CMOS electronics are produced at a commercial or otherwise standard foundry, and the resultant wafers are put through a post-processing etch step to create monolithic thermal pixel arrays (TPAs). A post-processing etch needs to completely isolate the heaters, and not affect the CMOS electronics in any way. The silicon etchant that was used as a method of thermal isolation was a tetra-methyl ammonium hydroxide (TMAH) solution. | | | |
| 14. SUBJECT TERMS Mission Area: Ocean Surveillance electronic devices metrology calibration | | | 15. NUMBER OF PAGES 28 |
| | | | 16. PRICE CODE |
| 17. SECURITY CLASSIFICATION OF REPORT UNCLASSIFIED | 18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED | 19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED | 20. LIMITATION OF ABSTRACT SAME AS REPORT |

| | | |
|--|---|---------------------------------------|
| 21a. NAME OF RESPONSIBLE INDIVIDUAL B. W. Offord | 21b. TELEPHONE (include Area Code) (619) 553-5503 e-mail: offord@spawar.navy.mil | 21c. OFFICE SYMBOL D876 |
| | | |

INITIAL DISTRIBUTION

| | | |
|-------|-------------------|------|
| D0012 | Patent Counsel | (1) |
| D0271 | Archive/Stock | (6) |
| D0274 | Library | (2) |
| D027 | M. E. Cathcart | (1) |
| D0271 | D. Richter | (1) |
| D712 | J. M. Weber | (4) |
| D7405 | D. N. Williams | (2) |
| D853 | R. L. Shimabukuro | (1) |
| D853 | S. D. Kasa | (1) |
| D87 | E. A. Engh | (1) |
| D876 | M. E. Aklufi | (5) |
| D876 | B. W. Offord | (10) |
| D876 | P. M. Sullivan | (5) |

Defense Technical Information Center
Fort Belvoir, VA 22060-6218 (4)

SSC San Diego Liaison Office
Arlington, VA 22202-4804

Center for Naval Analyses
Alexandria, VA 22302-0268

Navy Acquisition, Research and
Development Information Center
Arlington, VA 22202-3734

Government-Industry Data Exchange
Program Operations Center
Corona, CA 91718-8000